



ESD5302F

2-Lines, Uni-directional, Ultra-low Capacitance Transient Voltage Suppressors

Descriptions

The ESD5302F is an ultra-low capacitance TVS (Transient Voltage Suppressor) array designed to protect high speed data interfaces. It has been specifically designed to protect sensitive electronic components which are connected to data and transmission lines from over-stress caused by ESD (Electrostatic Discharge).

The ESD5302F incorporates two pairs of ultra- low capacitance steering diodes plus a TVS diode.

The ESD5302F may be used to provide ESD protection up to ±20kV (contact and air discharge) according to IEC61000-4-2, and withstand peak pulse current up to 4A (8/20µs) according to IEC61000-4-5.

The ESD5302F is available in SOT-23 package. Standard products are Pb-free and Halogen-free.

Features

- Stand-off voltage: 5V Max
- Transient protection for each line according to IEC61000-4-2 (ESD): ±20kV (contact and air discharge) IEC61000-4-4 (EFT): 40A (5/50ns) IEC61000-4-5 (surge): 4A (8/20µs)
- Ultra-low capacitance: C_J = 0.4pF typ.
- Ultra-low leakage current: I_R < 1nA typ.
- Low clamping voltage: V_{CL} = 20V @ I_{PP} = 16A(TLP)
- Solid-state silicon technology

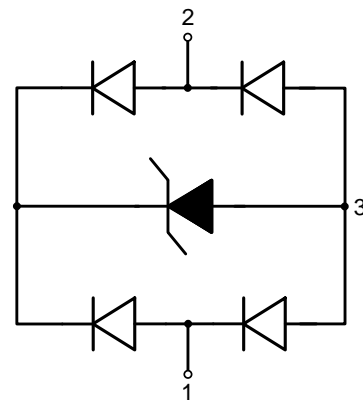
Applications

- USB 2.0 and USB 3.0
- HDMI 1.3 and HDMI 1.4
- SATA and eSATA
- DVI
- IEEE 1394
- PCI Express
- Portable Electronics
- Notebooks

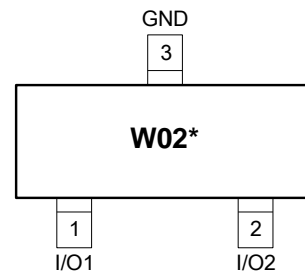
<http://www.cbcv.net>



SOT-23 (Top View)



Circuit diagram



W = Will
02 = Device code
* = Month code (A~Z)

Marking (Top View)

Order information

Device	Package	Shipping
ESD5302F-3/TR	SOT-23	3000/Tape&Reel

**Absolute maximum ratings**

Parameter	Symbol	Rating	Unit
Peak pulse power ($t_p = 8/20\mu s$)	P_{pk}	60	W
Peak pulse current ($t_p = 8/20\mu s$)	I_{PP}	4	A
ESD according to IEC61000-4-2 air discharge	V_{ESD}	± 20	kV
ESD according to IEC61000-4-2 contact discharge		± 20	
Junction temperature	T_J	125	$^{\circ}C$
Operating temperature	T_{OP}	-40~85	$^{\circ}C$
Lead temperature	T_L	260	$^{\circ}C$
Storage temperature	T_{STG}	-55~150	$^{\circ}C$

Electrical characteristics ($T_A=25^{\circ}C$, unless otherwise noted)

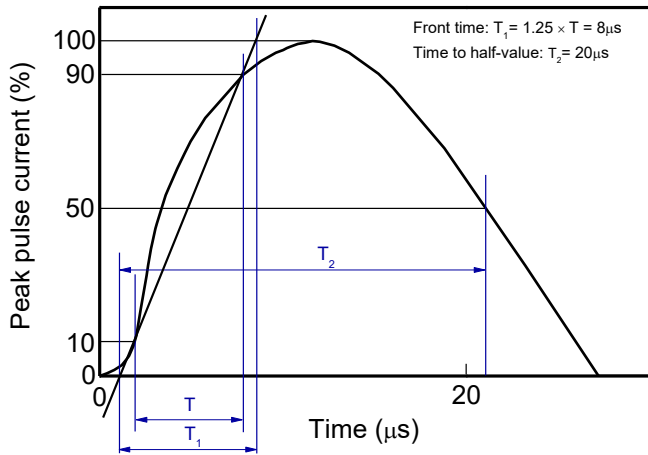
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Reverse maximum working voltage	V_{RWM}				5.0	V
Reverse leakage current	I_R	$V_{RWM} = 5V$		<1	100	nA
Reverse breakdown voltage	V_{BR}	$I_T = 1mA$	7.0	8.0	9.0	V
Forward voltage	V_F	$I_T = 10mA$	0.6	0.9	1.2	V
Clamping voltage ¹⁾	V_{CL}	$I_{PP} = 16A, t_p = 100ns$		20		V
Dynamic resistance ¹⁾	R_{DYN}			0.65		Ω
Clamping voltage ²⁾	V_{CL}	$I_{PP} = 1A, t_p = 8/20\mu s$			11	V
		$I_{PP} = 4A, t_p = 8/20\mu s$			15	V
Junction capacitance	C_J	$V_R = 0V, f = 1MHz$ Any I/O pin to GND		0.40	0.65	pF
		$V_R = 0V, f = 1MHz$ Between any I/O pin		0.25	0.40	pF

Notes:

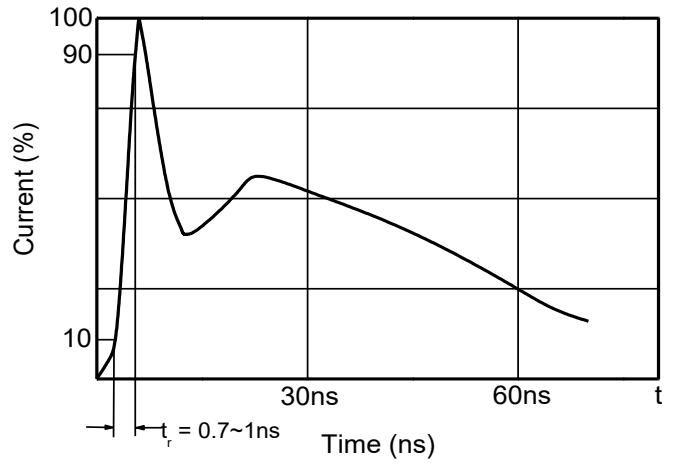
- 1) TLP parameter: $Z_0 = 50 \Omega$, $t_p = 100ns$, $t_r = 2ns$, averaging window from 60ns to 80ns. R_{DYN} is calculated from 4A to 16A.
- 2) According to IEC61000-4-5.



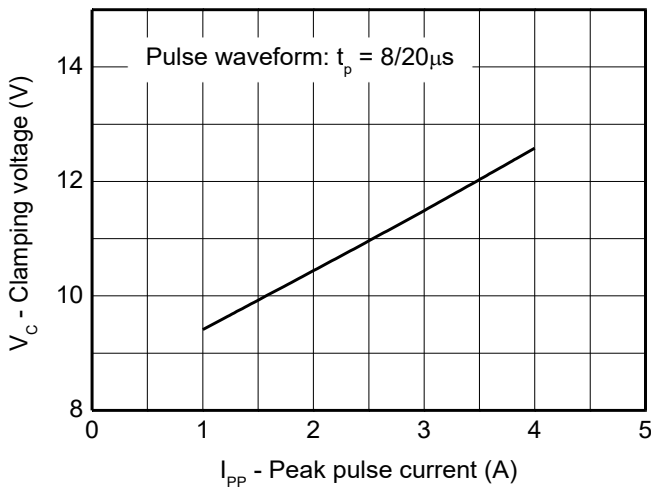
Typical characteristics ($T_A=25^\circ\text{C}$, unless otherwise noted)



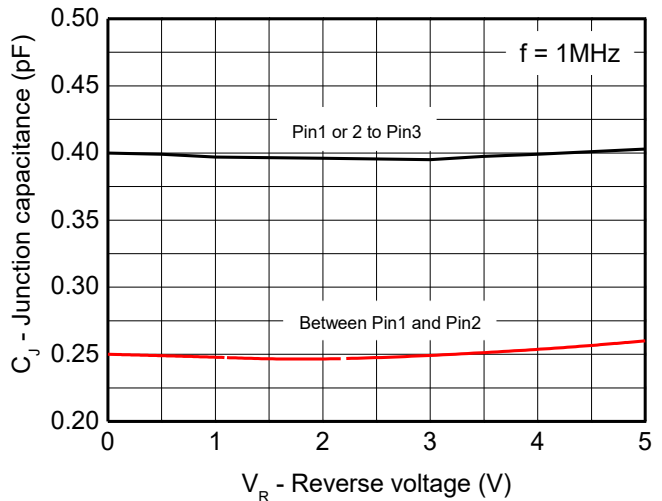
8/20μs waveform per IEC61000-4-5



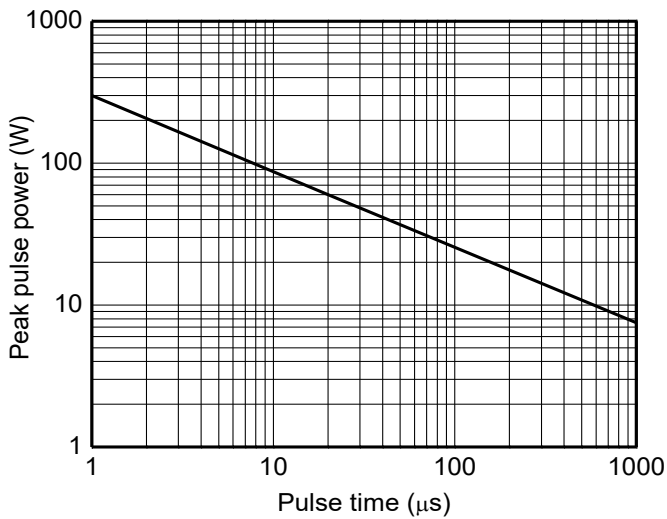
Contact discharge current waveform per IEC61000-4-2



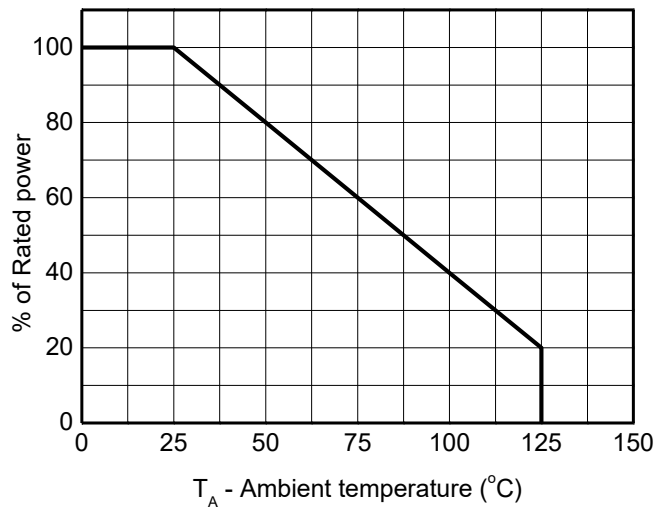
Clamping voltage vs. Peak pulse current



Capacitance vs. Reverse voltage



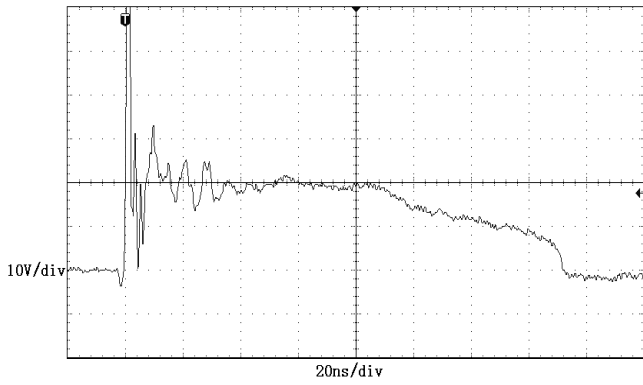
Non-repetitive peak pulse power vs. Pulse time



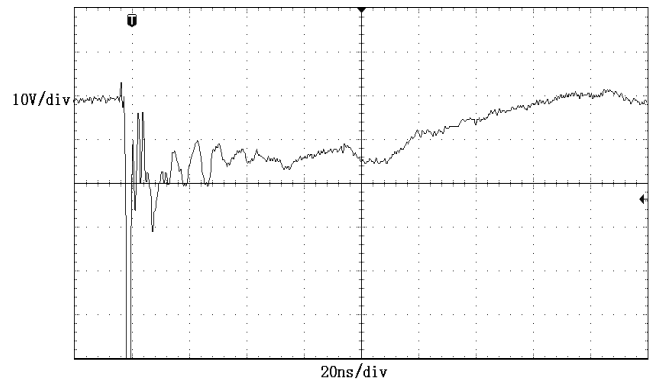
Power derating vs. Ambient temperature



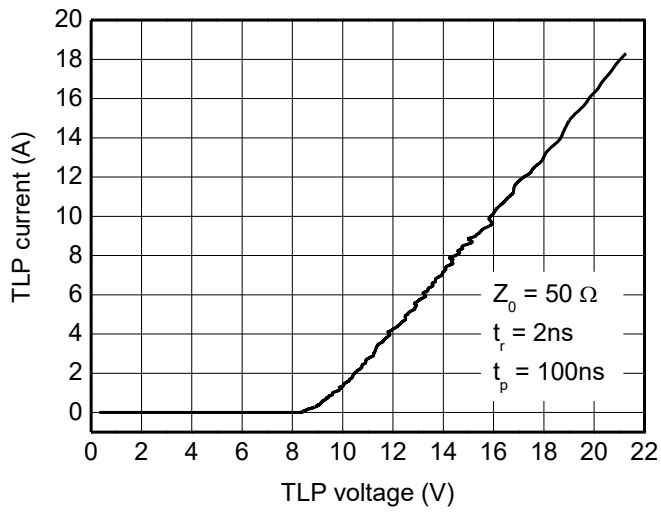
Typical characteristics ($T_A=25^\circ\text{C}$, unless otherwise noted)



ESD clamping
(+8kV contact discharge per IEC61000-4-2)



ESD clamping
(-8kV contact discharge per IEC61000-4-2)



TLP Measurement



Application Information

The ESD5302F is designed to protect two high speed line against ESD. Fig1 is shown the connection and Fig2 is shown PCB Layout guide for USB interface ESD protection

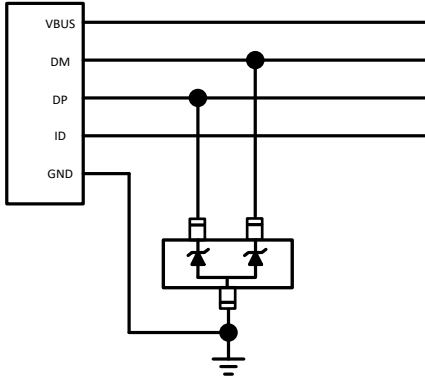


Fig1

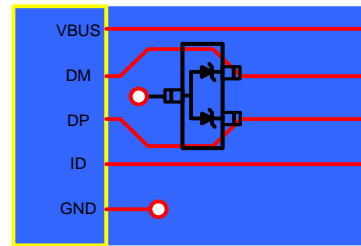
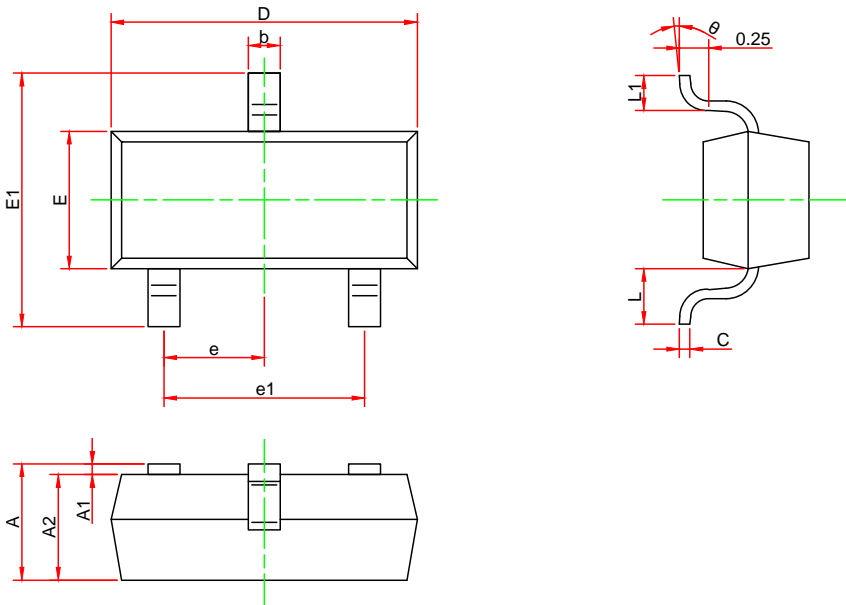


Fig2



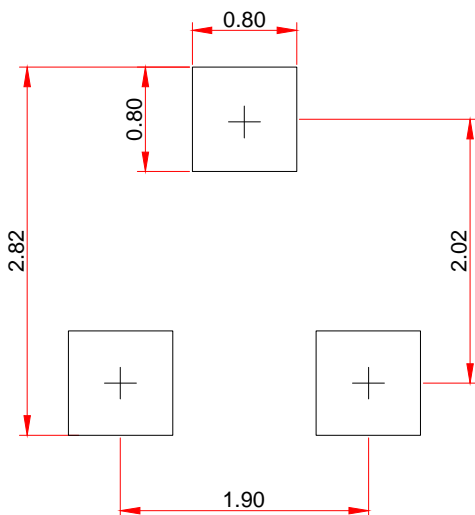
Package outline dimensions

SOT-23



Symbol	Dimensions in millimeters		
	Min.	Typ.	Max.
A	0.900	-	1.150
A1	0.000	-	0.100
A2	0.900	-	1.050
b	0.300	-	0.500
c	0.080	-	0.150
D	2.800	-	3.000
E	1.200	-	1.400
E1	2.250	-	2.550
e	0.950TYP		
e1	1.800	-	2.000
L	0.550REF		
L1	0.300	-	0.500
θ	0°	-	8°

Recommend land pattern (Unit: mm)



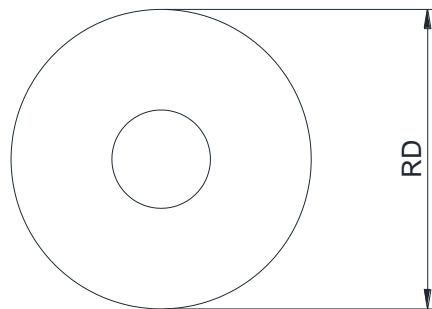
Notes:

This recommended land pattern is for reference purposes only. Please consult your manufacturing group to ensure your PCB design guidelines are met.

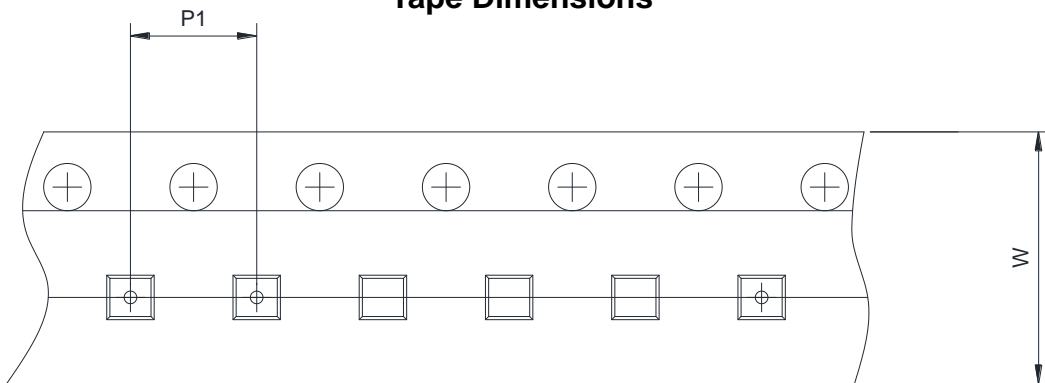


TAPE AND REEL INFORMATION

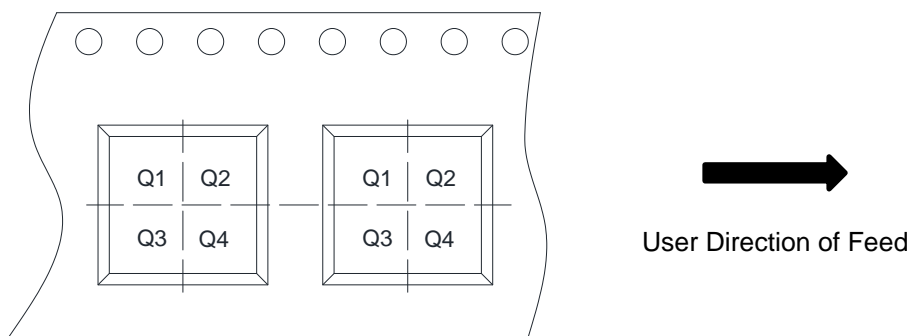
Reel Dimensions



Tape Dimensions



Quadrant Assignments For PIN1 Orientation In Tape



RD	Reel Dimension	<input checked="" type="checkbox"/> 7inch	<input type="checkbox"/> 13inch
W	Overall width of the carrier tape	<input checked="" type="checkbox"/> 8mm	<input type="checkbox"/> 12mm <input type="checkbox"/> 16mm
P1	Pitch between successive cavity centers	<input type="checkbox"/> 2mm	<input checked="" type="checkbox"/> 4mm <input type="checkbox"/> 8mm
Pin1	Pin1 Quadrant	<input type="checkbox"/> Q1	<input type="checkbox"/> Q2 <input checked="" type="checkbox"/> Q3 <input type="checkbox"/> Q4



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